

WHAT IS CLAIMED IS:

1 1. A method for providing a phase-locked loop with reduced
2 spurious tones, comprising:

3 comparing a reference clock signal to an internal clock
4 signal to generate a first signal;

5 sampling the first signal based on a sampling clock
6 signal to generate a second signal, the sampling clock signal
7 reduced with respect to the reference clock signal; and

8 generating the internal clock signal based on the second
9 signal.

1 2. The method of Claim 1, further comprising:

2 generating an up signal or a down signal based on the
3 comparison of the reference clock signal to the internal clock
4 signal;

5 generating a charge pump output signal based on the up
6 and down signals;

7 generating the first signal based on the charge pump
8 output signal;

9 generating an output frequency signal based on the second
10 signal; and

11 dividing the output frequency signal by a predetermined
12 amount to generate the internal clock signal.

1 3. The method of Claim 2, generating the charge pump output
2 signal comprising sourcing current based on the up signal and
3 sinking current based on the down signal, and generating the
4 stabilized signal comprising injecting currents into a
5 stabilization filter based on the up signal and draining currents
6 from the stabilization filter based on the down signal.

1 4. The method of Claim 3, further comprising generating a
2 loop filter output signal based on the second signal and generating
3 the output frequency signal based on the second signal comprising
4 generating the output frequency signal based on the loop filter
5 output signal.

1 5. The method of Claim 1, further comprising:
2 dividing a reference frequency signal by a predetermined
3 value, R , to generate the reference clock signal;
4 dividing the reference clock signal by a predetermined
5 value, D , to generate a reduced frequency signal; and
6 generating the sampling clock signal based on the reduced
7 frequency signal.

1 6. The method of Claim 5, generating the sampling clock
2 signal based on the reduced frequency signal comprising creating a
3 pulse based on the reduced frequency signal to generate a clock
4 signal and buffering the pulse to generate an inverted clock
5 signal.

1 7. The method of Claim 5, the predetermined amount
2 comprising one of N and $N+X/D$.

1 8. A method for providing a phase-locked loop with reduced
2 spurious tones, comprising:

3 dividing a reference clock signal by a predetermined
4 value, D, to generate a reduced frequency signal;

5 generating a sampling clock signal based on the reduced
6 frequency signal;

7 comparing the reference clock signal to an internal clock
8 signal;

9 generating an up signal or a down signal based on the
10 comparison of the reference clock signal to the internal clock
11 signal;

12 generating a charge pump output signal based on the up
13 and down signals;

14 generating a stabilized signal based on the charge pump
15 output signal;

16 sampling the stabilized signal based on the sampling
17 clock signal to generate a sampled output signal;

18 generating an output frequency signal based on the
19 sampled output signal; and

20 dividing the output frequency signal by a predetermined
21 amount to generate the internal clock signal.

1 9. The method of Claim 8, further comprising dividing a
2 reference frequency signal by a predetermined value, R, to generate
3 the reference clock signal.

1 10. The method of Claim 9, the predetermined amount
2 comprising one of N and $N+X/D$, D comprising about 15, N comprising
3 about 800, and R comprising about 10.

1 11. The method of Claim 8, generating the sampling clock
2 signal based on the reduced frequency signal comprising creating a
3 pulse based on the reduced frequency signal to generate a clock
4 signal and buffering the pulse to generate an inverted clock
5 signal.

1 12. The method of Claim 8, generating the charge pump output
2 signal comprising sourcing current based on the up signal and
3 sinking current based on the down signal.

1 13. The method of Claim 8, generating the stabilized signal
2 comprising injecting currents into a stabilization filter based on
3 the up signal and draining currents from the stabilization filter
4 based on the down signal.

1 14. The method of Claim 8, further comprising generating a
2 loop filter output signal based on the sampled output signal,
3 generating the output frequency signal based on the sampled output
4 signal comprising generating the output frequency signal based on
5 the loop filter output signal.

1 15. A phase-locked loop, comprising:

2 a spur reduction circuit operable to receive a reference
3 clock signal and to divide the reference clock signal by a
4 predetermined value, D, to generate a reduced frequency signal;

5 a clock/buffer circuit coupled to the spur reduction
6 circuit, the clock/buffer circuit operable to generate a sampling
7 clock signal based on the reduced frequency signal;

8 a phase detector operable to compare the reference clock
9 signal to an internal clock signal to generate an up signal or a
10 down signal;

11 a charge pump coupled to the phase detector, the charge
12 pump operable to generate a charge pump output signal based on the
13 up and down signals;

14 a stabilization filter coupled to the charge pump, the
15 stabilization filter operable to generate a stabilized signal based
16 on the charge pump output signal;

17 a sampling circuit coupled to the stabilization filter
18 and to the clock/buffer circuit, the sampling circuit operable to
19 sample the stabilized signal based on the sampling clock signal to
20 generate a sampled output signal;

21 an oscillator coupled to the sampling circuit, the
22 oscillator operable to generate an output frequency signal based on
23 the sampled output signal; and

24 a feedback divider coupled between the oscillator and the
25 phase detector, the feedback divider operable to divide the output
26 frequency signal by a predetermined amount to generate the internal
27 clock signal.

1 16. The phase-locked loop of Claim 15, further comprising an
2 input divider coupled to the phase detector and to the spur
3 reduction circuit, the input divider operable to divide a reference
4 frequency signal by a predetermined value, R , to generate the
5 reference clock signal.

1 17. The phase-locked loop of Claim 16, the predetermined
2 amount comprising one of N and $N+X/D$, D comprising about 15, N
3 comprising about 800, and R comprising about 10.

1 18. The phase-locked loop of Claim 15, the clock/buffer
2 circuit operable to generate the sampling clock signal by creating
3 a pulse based on the reduced frequency signal to generate a clock
4 signal, inverting the pulse to generate an inverted clock signal,
5 and buffering the clock signal and the inverted clock signal.

1 19. The phase-locked loop of Claim 18, the sampling circuit
2 comprising an n-channel transistor, a p-channel transistor and a
3 hold capacitor, the n-channel transistor comprising a gate operable
4 to receive the clock signal and the p-channel transistor comprising
5 a gate operable to receive the inverted clock signal.

1 20. The phase-locked loop of Claim 15, further comprising a
2 low pass filter coupled between the sampling circuit and the
3 oscillator, the low pass filter operable to generate a loop filter
4 output signal based on the sampled output signal, the oscillator
5 operable to generate the output frequency signal based on the loop
6 filter output signal.